CLAIMS

1. A method of executing a refresh operation in a synchronous memory device receiving an external clock signal, the method comprising:

initiating at least one refresh operation in the memory device; and

ceasing generation of an internal clock signal timed with respect to the external clock signal for at least a portion of the time in which at least one refresh operation takes to complete.

2. The method of claim 1 wherein initiating at least one refresh operation comprises initiating n refresh operations and ceasing generation of the internal clock signal comprises ceasing generation of the internal clock signal once for every n refresh operations.

3. The method of claim 1 wherein ceasing generation of the internal clock signal comprises ceasing generation of the internal clock signal for at least a portion of the time a refresh operation takes to complete for every refresh operation executed.

4. The method of claim 1 wherein the refresh operation takes a refresh time period to complete, the refresh operation comprising an internal refresh operation time period during which the refresh operation completes internally and further comprises a precharge time period, and wherein ceasing generation of the internal clock signal for at least a portion of the time in which at least one refresh operation takes to complete comprises ceasing generation of the internal clock signal for the duration of the internal refresh operation time period.

5. The method of claim 4, further comprises resuming generation of the internal clock signal after the refresh operation time period elapses and monitoring operation conditions in the synchronous memory device during the precharge time period for changes from

when generation of the internal clock signal ceased and when generation of the internal clock signal resumed.

6. The method of claim 1 wherein ceasing generation of the internal clock signal comprises idling a synchronizing clock circuit in the synchronous memory device.

7. The method of claim 6, further comprising idling output circuitry operating in response to the internal clock signal.

8. The method of claim 6 wherein the synchronizing clock circuit comprises a delay-locked loop.

9. The method of claim 1 wherein the refresh operation comprises an auto-refresh operation.

10. A method of executing a refresh operation in a memory device, comprising:

initiating a refresh operation having a refresh time period in which the refresh operation is completed and which elapses before execution of a new memory command can begin;

idling a synchronizing clock circuit in the memory device for at least a portion of the refresh time period, the synchronizing clock circuit generating an output clock signal in synchronicity with an input clock signal when enabled; and

re-enabling the synchronizing clock circuit prior to the refresh time period elapsing.

11. The method of claim 10, further comprising generating a refresh execution signal in response to the memory device receiving a refresh command and wherein idling the

synchronizing clock circuit comprises idling the synchronizing clock circuit in response to the refresh execution signal becoming active and re-enabling the synchronizing clock circuit comprises re-enabling the synchronizing clock circuit in response to the refresh execution signal becoming inactive.

12. The method of claim 10, further comprising monitoring operating conditions in the memory device by the synchronizing clock circuit subsequent to re-enabling and adjusting timing of the synchronizing clock circuit when the operation conditions have changed from when the synchronizing clock circuit is idled to when the synchronizing clock circuit is re-enabled.

13. The method of claim 10 wherein idling the synchronizing clock circuit comprises ceasing generation of an internal clock signal.

14. The method of claim 13, further comprising idling output circuitry operating in response to the internal clock signal.

15. The method of claim 10 wherein the refresh operation comprises an auto refresh operation.

16. The method of claim 10 wherein the synchronizing clock circuit comprises a delay-locked loop.

17. The method of claim 10 wherein the refresh time period comprises an internal refresh operation time period during which the refresh operation completes internally and further comprises a precharge time period, and wherein re-enabling the synchronizing clock circuit comprises re-enabling the synchronizing clock circuit after the internal refresh operation time period elapses.

18. A method for executing a refresh operation in a memory device, comprising:

initiating a plurality of refresh operations;

for every n refresh operations initiated, idling a synchronizing clock circuit for at least a portion of a time period taken for one refresh operation to complete; and

and enabling the synchronizing clock circuit for the remaining (n-1) refresh operations.

19. The method of claim 18 wherein the plurality of refresh operations are initiated in sequence.

20. The method of claim 18 wherein n refresh operations are initiated in sequence.

21. The method of claim 18, further comprising generating a refresh execution signal in response to the memory device receiving a refresh command and wherein idling the synchronizing clock circuit comprises idling the synchronizing clock circuit in response to the refresh execution signal for the one refresh operation becoming active and re-enabling the synchronizing clock circuit comprises re-enabling the synchronizing clock circuit in response to the refresh execution signal for the one refresh operation becoming inactive.

22. The method of claim 18, further comprising monitoring operating conditions in the memory device by the synchronizing clock circuit subsequent to being enabled and adjusting timing of the synchronizing clock circuit when the operation conditions have changed from when the synchronizing clock circuit is idled to when the synchronizing clock circuit is enabled.

23. The method of claim 18 wherein idling the synchronizing clock circuit comprises ceasing generation of an internal clock signal.

24. The method of claim 23, further comprising for every n refresh operations, idling output circuitry operating in response to the internal clock signal.

25. The method of claim 18 wherein the refresh operation comprises an auto refresh operation.

26. The method of claim 18 wherein the synchronizing clock circuit comprises a delay-locked loop.

27. The method of claim 18 wherein each refresh operation takes a refresh time period to elapse before a new memory command can be executed, the refresh time period comprises an internal refresh operation time period during which the refresh operation completes internally and further comprises a precharge time period, and wherein enabling the synchronizing clock circuit comprises enabling the synchronizing clock circuit after the internal refresh operation time period of the one refresh operation elapses.

28. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

a refresh circuit coupled to the memory-cell array and the control circuit to execute a refresh operation having a refresh time period in which the refresh operation is completed and which elapses before execution of a new memory command begin in response to a refresh command signal provided by the control circuit;

a synchronizing clock circuit coupled to the control circuit and receiving an input clock signal, the synchronizing clock circuit operable to generate an internal clock signal timed with respect to the input clock signal; and

a synchronizing clock control circuit coupled to the synchronizing clock circuit and the control circuit, the synchronizing clock control circuit operable to generate an idle signal in response to the refresh command signal to idle the synchronizing clock circuit for at least a portion of the refresh time period.

29. The memory device of claim 28 wherein the synchronizing clock circuit comprises a delay-locked loop.

30. The memory device of claim 28 wherein the synchronizing clock control circuit comprises an OR logic gate having a first input coupled to the control circuit to receive the refresh command signal and a second input coupled to the control circuit to receive a power-down signal, the OR logic gate further having an output coupled to the synchronizing clock circuit to provide the idle signal.

31. The memory device of claim 28 wherein the synchronizing clock control circuit comprises:

a counter circuit having an input coupled to the control circuit to receive the refresh command signal, the counter circuit operable to generate an active output signal at an output in response to counting n active refresh command signals an AND logic gate having a first input coupled to the control circuit to receive the refresh command signal and a second input coupled to the output of the counter circuit and further having an output; and

an OR logic gate having a first input coupled to the output of the AND logic gate and a second input coupled to the control circuit to receive a power-down signal, the OR logic gate further having an output coupled to the synchronizing clock circuit to provide the idle signal.

32. The memory device of claim 28 wherein the read/write circuit comprises output circuitry coupled to the synchronizing clock circuit to output data from the memory-cell array in response to the internal clock signal.

33. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

a refresh circuit coupled to the memory-cell array and the control circuit to execute a refresh operation refreshing memory cells of the memory-cell array in response to a refresh command signal provided by the control circuit;

a synchronizing clock circuit coupled to the control circuit and receiving an input clock signal, the synchronizing clock circuit operable to generate an internal clock signal timed with respect to the input clock signal; and a synchronizing clock control circuit coupled to the synchronizing clock circuit and the control circuit, the synchronizing clock control circuit operable to generate an idle signal in response to receiving n refresh command signals to idle the synchronizing clock circuit for at least a portion of one refresh time period for every n refresh operations.

34. The memory device of claim 33 wherein the synchronizing clock control circuit comprises:

a counter circuit having an input coupled to the control circuit to receive the refresh command signal, the counter circuit operable to generate an active output signal at an output in response to counting n active refresh command signals

an AND logic gate having a first input coupled to the control circuit to receive the refresh command signal and a second input coupled to the output of the counter circuit and further having an output; and

an OR logic gate having a first input coupled to the output of the AND logic gate and a second input coupled to the control circuit to receive a power-down signal, the OR logic gate further having an output coupled to the synchronizing clock circuit to provide the idle signal.

35. The memory device of claim 33 wherein the synchronizing clock circuit comprises a delay-locked loop.

36. The memory device of claim 33 wherein the read/write circuit comprises output circuitry coupled to the synchronizing clock circuit to output data from the memory-cell array in response to the internal clock signal.

37. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

a refresh circuit coupled to the memory-cell array and the control circuit to execute a refresh operation having a refresh time period in which the refresh operation is completed and which elapses before execution of a new memory command begin in response to a refresh command signal provided by the control circuit;

a synchronizing clock circuit coupled to the control circuit and receiving an input clock signal, the synchronizing clock circuit operable to generate an internal clock signal timed with respect to the input clock signal; and

a synchronizing clock control circuit coupled to the synchronizing clock circuit and the control circuit, the synchronizing clock control circuit operable to generate an idle signal in response to the refresh command signal to idle the synchronizing clock circuit for at least a portion of the refresh time period.

38. The processor-based system of claim 37 wherein the synchronizing clock circuit of the memory device comprises a delay-locked loop.

39. The processor-based system of claim 37 wherein the synchronizing clock control circuit of the memory device comprises an OR logic gate having a first input coupled to the control circuit to receive the refresh command signal and a second input coupled to the control circuit to receive a power-down signal, the OR logic gate further having an output coupled to the synchronizing clock circuit to provide the idle signal.

40. The processor-based system of claim 37 wherein the synchronizing clock control circuit of the memory device comprises:

a counter circuit having an input coupled to the control circuit to receive the refresh command signal, the counter circuit operable to generate an active output signal at an output in response to counting n active refresh command signals

an AND logic gate having a first input coupled to the control circuit to receive the refresh command signal and a second input coupled to the output of the counter circuit and further having an output; and

an OR logic gate having a first input coupled to the output of the AND logic gate and a second input coupled to the control circuit to receive a power-down signal, the OR logic gate further having an output coupled to the synchronizing clock circuit to provide the idle signal.

41. The processor-based system of claim 37 wherein the read/write circuit of the memory device comprises output circuitry coupled to the synchronizing clock circuit to output data from the memory-cell array in response to the internal clock signal.

42. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

a refresh circuit coupled to the memory-cell array and the control circuit to execute a refresh operation refreshing memory cells of the memory-cell array in response to a refresh command signal provided by the control circuit;

a synchronizing clock circuit coupled to the control circuit and receiving an input clock signal, the synchronizing clock circuit operable to generate an internal clock signal timed with respect to the input clock signal; and

a synchronizing clock control circuit coupled to the synchronizing clock circuit and the control circuit, the synchronizing clock control circuit operable to generate an idle signal in response to receiving n refresh command signals to idle the synchronizing clock circuit for at least a portion of one refresh time period for every n refresh operations.

43. The processor-based system of claim 42 wherein the synchronizing clock control circuit of the memory device comprises:

a counter circuit having an input coupled to the control circuit to receive the refresh command signal, the counter circuit operable to generate an active output signal at an output in response to counting n active refresh command signals

an AND logic gate having a first input coupled to the control circuit to receive the refresh command signal and a second input coupled to the output of the counter circuit and further having an output; and

an OR logic gate having a first input coupled to the output of the AND logic gate and a second input coupled to the control circuit to receive a power-down signal, the OR logic gate further having an output coupled to the synchronizing clock circuit to provide the idle signal.

44. The processor-based system of claim 42 wherein the synchronizing clock circuit of the memory device comprises a delay-locked loop.

45. The processor-based system of claim 42 wherein the read/write circuit of the memory device comprises output circuitry coupled to the synchronizing clock circuit to output data from the memory-cell array in response to the internal clock signal.